What Is Claimed Is:

1. A memory device comprising:

an erasable and writable nonvolatile memory; and

a control circuit,

wherein said control circuit is enabled to perform replacement processing of memory areas at a prescribed timing, and

wherein said replacement processing is accomplished by writing stored data in a first memory area in which rewriting is relatively infrequent into an unused second memory area, and making the second memory area into which the writing has been done a used area in place of said first memory area.

2. The memory device according to Claim 1,

wherein said memory area holds rewrite frequency data, and

wherein said control circuit references rewrite frequency data obtained from each of a group of memory areas and searches them for said first memory area.

3. The memory device according to Claim 1,

wherein said nonvolatile memory is provided in each of its memory areas with a storage area for a distinguishing flag indicating whether or not the area is unused, and

wherein said control circuit references said distinguishing flag to search for said unused second memory area.

4. The memory device according to Claim 1,

wherein said memory area holds rewrite frequency data, and

wherein said control circuit references the rewrite frequency data to search for a memory area in which rewriting is more frequent than in said first memory area and to make it said second memory area.

5. The memory device according to Claim 1,

wherein said control circuit performs said replacement processing in response to a specific command.

6. The memory device according to Claim 1,

wherein said control circuit performs said replacement processing in response to completion of processing of a specific command.

7. The memory device according to Claim 1,

wherein, in the event of an instruction by another command after a start of said replacement processing, the ongoing replacement processing is abandoned to give priority to processing of that other command.

8. The memory device according to Claim 1,

wherein said control circuit performs said replacement processing in response to arrival of a frequency of rewriting into the nonvolatile memory at a prescribed number of times.

9. A memory device comprising:

an erasable and writable nonvolatile memory; and

a control circuit,

wherein said control circuit is enabled to perform

replacement processing of memory areas at a prescribed timing, and

wherein said replacement processing is accomplished by replacing with a prescribed unused memory area a prescribed used memory area in which rewriting is less frequent than in the prescribed unused memory area.

10. A memory device comprising:

an erasable and writable nonvolatile memory; and

a control circuit,

wherein said control circuit is enabled to perform replacement processing of memory areas at a prescribed timing, and

wherein said replacement processing is accomplished by replacing a prescribed memory area with another in which rewriting is less frequent than that prescribed memory area and placing said other memory area in an unused state while said prescribed memory area after the replacement is being used.

11. A memory device comprising:

an erasable and writable nonvolatile memory; and

a control circuit,

wherein said nonvolatile memory has an unused area distinguishing table for storing a distinguishing flag which indicates whether or not any memory area is an unused area,

wherein said control circuit, in write processing, makes one of the unused memory areas indicated by said distinguishing

flag the destination for data writing and is enabled to perform replacement processing at a prescribed timing on the used memory area indicated by said distinguishing flag, and

wherein said replacement processing is accomplished by writing stored data in a first memory area in which rewriting is relatively infrequent into an unused second memory area, and making the second memory area into which the writing has been done a used area in place of said first memory area.

12. The memory device according to Claim 11,

wherein said nonvolatile memory has a used address registration table for registering, matched with logical addresses, physical addresses of memory areas to be used, and

wherein said control circuit, when altering the distinguishing flag to an unused area, invalidates the matching between the memory area allocated to the distinguishing flag and the physical address and, when altering the distinguishing flag to a used area, matches the memory area allocated to the distinguishing flag with a prescribed physical address.

13. The memory device according to Claim 12,

wherein said control circuit, when it is to replace one memory area with another memory area to alter it into a used area, performs processing, before causing the matching between the logical address and the physical address pertaining to that alteration to be reflected in the used address registration table on said nonvolatile memory, to cause the distinguishing flag for said one memory area

to be altered from an unused area to a used area to be reflected in the unused area distinguishing table on said nonvolatile memory and performs processing, after the matching has been reflected in said used address registration table, to cause the distinguishing flag for said other memory area to be altered from a used area into an unused area to be reflected in the unused area distinguishing table on said nonvolatile memory.

14. The memory device according to Claim 12,

wherein said memory area holds rewrite frequency data, and

wherein said control circuit references rewrite frequency data obtained from each of a group of memory areas and searches them for said first memory area.

15. The memory device according to Claim 12,

wherein said control circuit references said distinguishing flag to search for said unused second memory area.

16. The memory device according to Claim 12,

wherein said control circuit references the rewrite frequency data to search for a memory area in which rewriting is more frequent than in said first memory area and to make it said second memory area.